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ARTICLE

Tunable Negative Differential Resistance in van der Waals Heterostructures at Room Temperature by Tailoring the Interface

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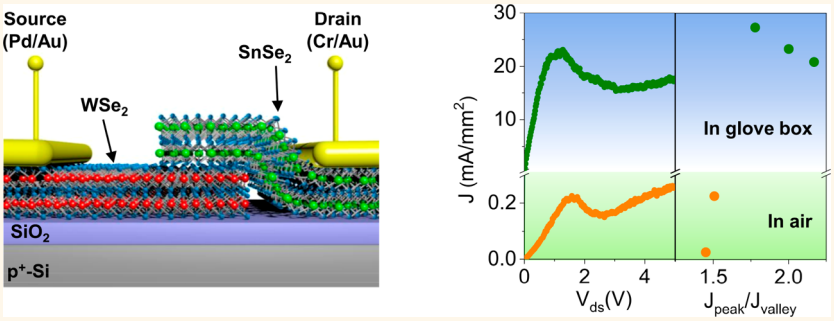
Supporting Information



ABSTRACT: **Vertically stacked two-dimensional van der Waals (vdW) heterostructures, used to obtain homogeneity and band steepness at interfaces, exhibit promising performance for band-to-band tunneling (BTBT) devices. Esaki tunnel diodes based on vdW heterostructures, however, yield poor current density and peak-to-valley ratio, inferior to those of three-dimensional materials. Here, we report the negative differential resistance (NDR) behavior in a $WSe_2/SnSe_2$ heterostructure system at room temperature and demonstrate that heterointerface control is one of the keys to achieving high device performance by constructing $WSe_2/SnSe_2$ heterostructures in inert gas environments. While devices fabricated in ambient conditions show poor device performance due to the observed oxidation layer at the interface, devices fabricated in inert gas exhibit extremely high peak current density up to 1460 mA/mm^2, 3−4 orders of magnitude higher than reported vdW heterostructure-based tunnel diodes, with a peak-to-valley ratio of more than 4 at room temperature. Besides, Pd/WSe_2 contact in our device possesses a much higher Schottky barrier than previously reported Cr/WSe_2 contact in the $WSe_2/SnSe_2$ device, which suppresses the thermionic emission current to less than the BTBT current level, enabling the observation of NDR at room temperature. Diode behavior can be further modulated by controlling the electrostatic doping and the tunneling barrier as well.**

KEYWORDS: *2D tunneling heterojunction, Esaki diode, negative differential resistance, tin diselenide, tungsten diselenide*

Esaki tunnel diodes or negative differential resistance (NDR) devices take advantage of quantum mechanical tunneling through a heavily doped p−n junction, in which charge carriers transfer from one energy band to another.[1,2] Having an NDR region, tunnel diodes show great potential for applications in oscillators, high-frequency amplifiers, and multivalued logics.[3−7] Besides, device operation originating from the majority-carrier tunnel rather than the minority-carrier storage endows Esaki diodes with high-speed capability, which is extremely desirable for low-power operation at room temperature.[8−14] To achieve more efficient tunneling in tunnel devices, the screening tunneling length (depletion width), governed by doping concentration, should be minimized. Tunnel devices based on traditional silicon or germanium are not tenable for controlling an abrupt doping profile of homojunctions at the sub-nanometer scale to reduce screening tunneling length.[15,16] Three-dimensional (3D) heterojunctions also suffer from complexity of the multiple quantum well structure and growth of III−V materials using molecular beam epitaxy or metal organic chemical vapor deposition, which are not easily accessible for integration.[17−19]

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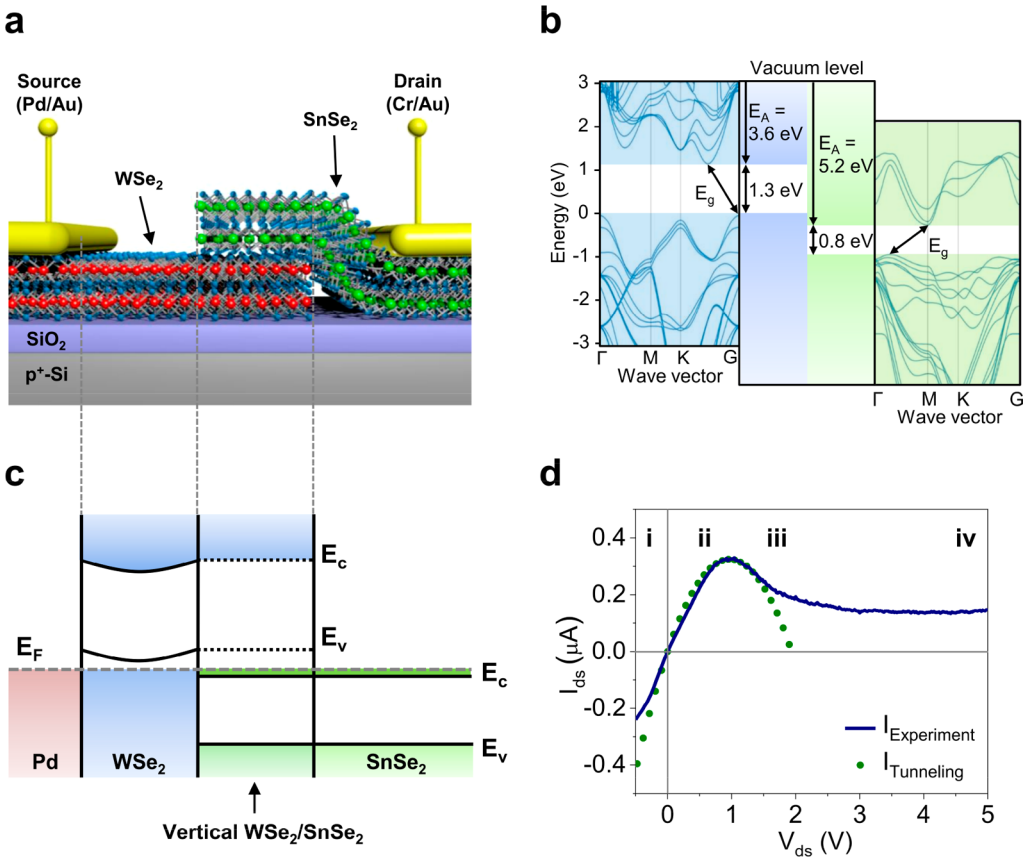

Figure 1. Device structure and NDR characteristic of a $WSe_2/SnSe_2$ Esaki diode. (a) Schematic of a two-terminal diode with p-type WSe_2 and n-type $SnSe_2$. (b) Band structures of WSe_2 and $SnSe_2$ with their electron affinities and band gaps obtained from our DFT calculation, suggesting initial type III, broken-gap band alignment in the heterostructure. (c) Band alignment simulation of the heterostructure with palladium contact, where a heavily p^+-n^+ junction appears in the planar direction. E_c, E_v, and E_f represent the conduction band, valence band, and the Fermi level, respectively. (d) Experimental measurement and theoretical fitting of the $I_{ds}-V_{ds}$ characteristic of the device fabricated under ambient conditions. The device is gated at −70 V.

Two-dimensional (2D) materials are promising substitutes due to their steep band edges and atomically thin nature with an absence of dangling bonds at the surface.[20−22] Furthermore, 2D materials are available on a wafer scale for integration.[23−25] Moreover, 2D layered semiconductors possess different electron affinities and a wide range of band gaps from 0.4 to 2.0 eV, allowing for the formation of diverse ultrathin stacks with type II (staggered gap) or type III (broken gap) band alignment.[22,26−29] With a sharp homogeneous band edge and a narrow screening tunneling length (van der Waals (vdW) gap), vdW heterostructure-based Esaki diodes thus offer high performance such as high current density and a high peak-to-valley ratio. However, all previously reported Esaki diodes using 2D layered materials show much lower device performance than 3D semiconductor diodes, consequently hindering their further application to band-to-band tunneling (BTBT) devices.[30−34]

RESULTS AND DISCUSSION

We first demonstrate that control of a sharp and clean vdW heterointerface is critical for achieving high-performance tunnel devices. An Esaki tunnel diode is based on vertically stacked $WSe_2/SnSe_2$ heterojunctions (Figure 1a, and for the fabrication process and characterization, see SI Notes 1 and 2 and Figures S1 and S2). The energy levels of WSe_2 and $SnSe_2$ calculated by density functional theory (Figure 1b and see SI Note 3)[35] depict the valence band edge of WSe_2 as higher than the conduction band edge of $SnSe_2$ by 0.3 eV, suggesting an initial type III, broken-gap alignment. As confirmed by the transfer characteristics of $SnSe_2$-FET and WSe_2-FET (see SI Note 4 and Figure S3), $SnSe_2$ is heavily n-doped and WSe_2 is ambipolar with palladium (Pd) contact. Accordingly, band alignments of $WSe_2/SnSe_2$ in contact with Pd are simulated using Poisson's equation (see SI Note 5 and Figure S5). Large differences in work function between Pd (~5.3 eV), $SnSe_2$, and WSe_2 induce the strong accumulation of hole carriers in WSe_2 to evolve the system into its thermal equilibrium. Band bending in WSe_2 takes place outside the overlapped $WSe_2/SnSe_2$ and in the planar direction instead of a vertical junction due to the thin thickness of WSe_2 (less than 10 nm).[7] Thus, a heavily doped p^+-n^+ lateral heterojunction with a broken gap is achieved (Figure 1c), establishing the BTBT channel for electrons.

Output characteristics of the device fabricated in air clearly exhibit the NDR behavior at room temperature (Figure 1d). $I_{ds}-V_{ds}$ curves of $SnSe_2$-FET and WSe_2-FET (see Figure S4) reveal that $SnSe_2$ is in ohmic contact with chromium metal, while a Schottky barrier exists in WSe_2/Pd contact, indicating that our NDR behavior primarily stems from the $p^+(WSe_2)-n^+(SnSe_2)$ heterojunction rather than the semiconductor–metal junction. As fitted by the theoretical calculation (Figure 1d, and for equation, see SI Note 6), I_{ds} is dominated by BTBT

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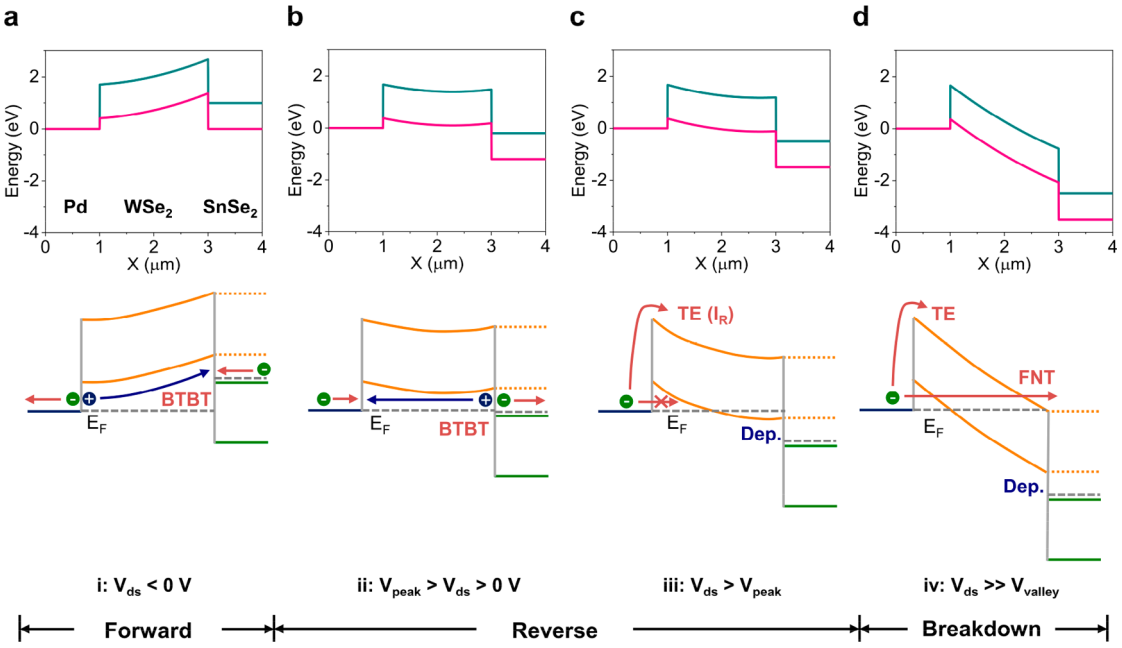

Figure 2. Band alignment simulations of Pd/WSe_2/$SnSe_2$ under different V_{ds} and the corresponding energy band diagrams. (a) Under the forward V_{ds}, electrons tunnel from $SnSe_2$ into WSe_2 and eventually flow into the Pd terminal. BTBT denotes the band-to-band tunneling. (b) Driven by a small reverse V_{ds}, electrons from the Pd source flow into WSe_2 and then tunnel into $SnSe_2$. (c) Further increase of the reverse V_{ds} induces the depletion of WSe_2, and thus electron tunneling is decreased. In this case, the thermionic emission starts to dominate I_{ds} with a saturated reverse current of I_R. The depletion of WSe_2 near the WSe_2/$SnSe_2$ junction is denoted as Dep. (d) Under a large reverse V_{ds}, the electron transport property turns into the FN tunneling or thermionic emission mechanism.

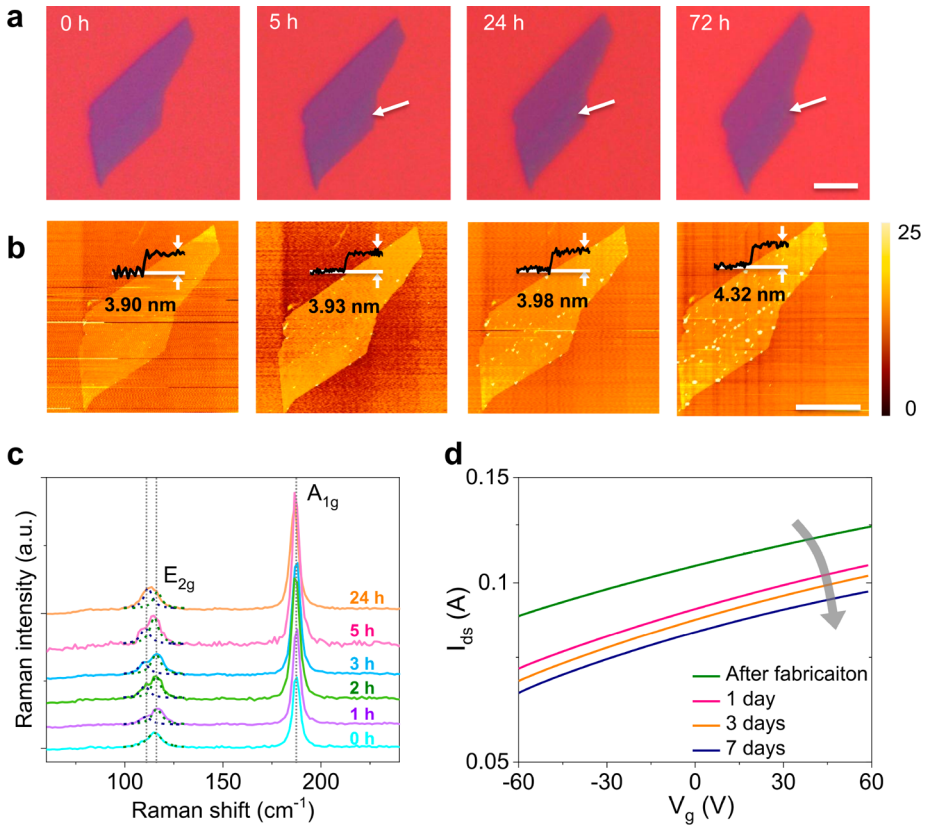

Figure 3. Oxidative degradation of an exfoliated $SnSe_2$ flake over time. (a) Optical images and (b) AFM mappings with extracted height profiles measured at 0, 5, 24, and 72 h. The scale bar is 5 μm. (c) Raman spectra acquired at 0, 1, 2, 3, 5, and 24 h. (d) I_{ds}–V_g curve of $SnSe_2$-FET measured after fabrication, 1 day, 3 days, and 7 days. V_{ds} for measurements is kept at 0.5 V.

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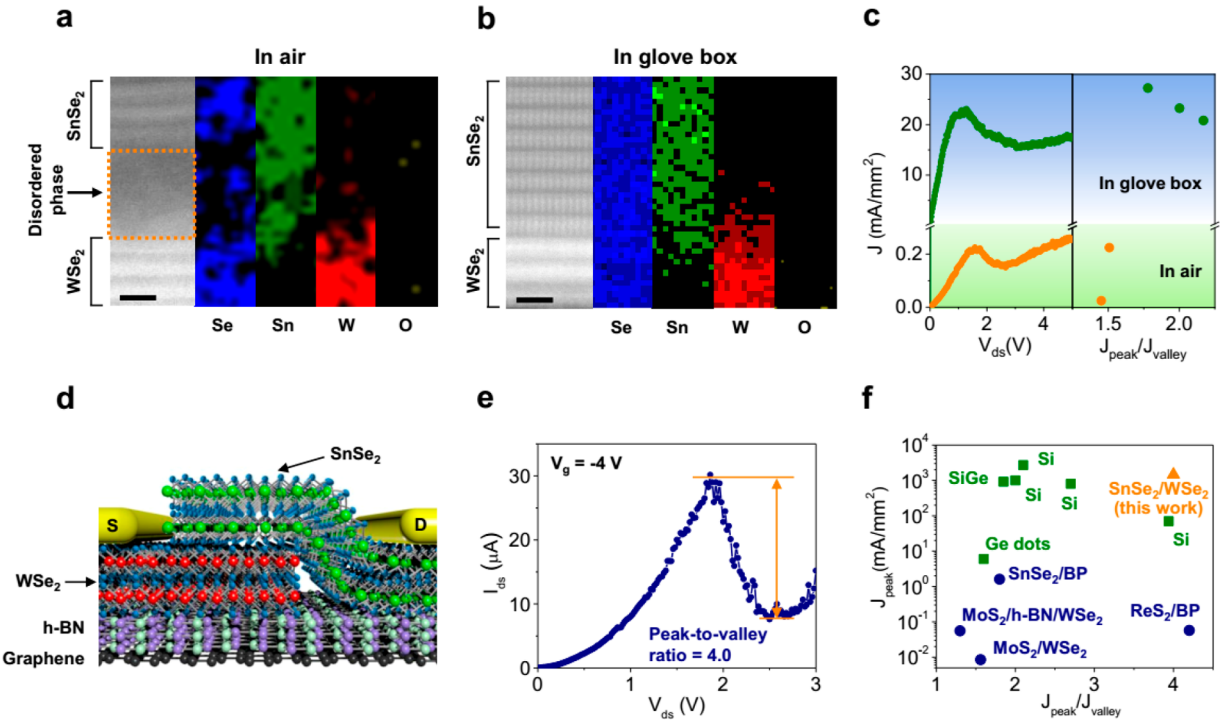

Figure 4. Improved NDR behavior of device fabricated in an inert gas environment and on an h-BN dielectric. Cross-sectional TEM images assisted with EDS element mappings of the device fabricated (a) in air and (b) in inert gas. The scale bar is 1 nm. (c) NDR behavior of devices fabricated on the SiO_2 dielectric in each environment at room temperature (left) and the reproducibility (right). All devices are operated at a back gate of −100 V. (d) Schematic of the NDR device fabricated on the h-BN dielectric layer and bottom monolayer graphene serving as the back-gate electrode. (e) High NDR performance with the peak-to-valley ratio of 4.0 and peak current of 30 μA (overlap area of 20.5 μm^2 in the p−n junction). (f) Performance comparison of our NDR device with other previously reported devices fabricated with traditional 2D materials (circles) and 3D semiconductors (squares).

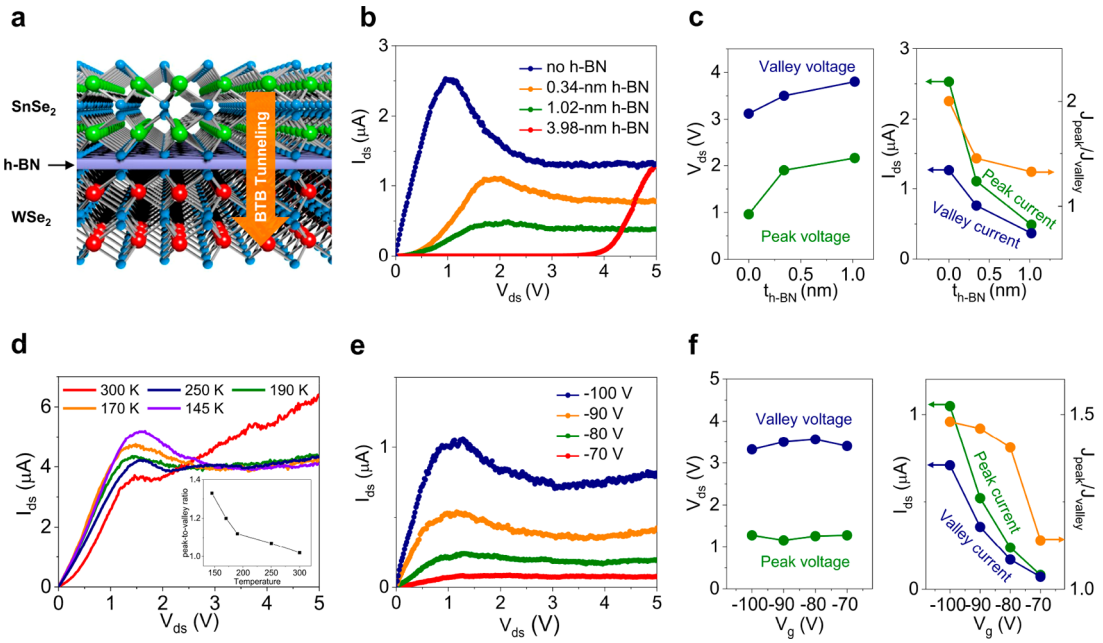

Figure 5. Tunable NDR behavior via the h-BN tunneling barrier and electrostatic doping. (a) Schematic of the h-BN layer as the tunneling barrier between WSe_2 and $SnSe_2$ layers. (b) NDR performance with different h-BN thicknesses. All devices are fabricated on the SiO_2 dielectric and operated at the back gate of −80 V. (c) Extracted peak and valley voltages (left) and peak and valley currents together with the peak-to-valley ratio (J_{peak}/ J_{valley}) (right) as a function of h-BN thickness. (d) NDR behavior at different temperatures. (e) NDR behavior under different back-gate biases. (f) Extracted peak and valley voltages (left) and peak and valley currents together with the peak-to-valley ratio (J_{peak}/ J_{valley}) (right) as a function of gate bias.

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current under negative V_{ds} and small positive V_{ds}. To further investigate the mechanism, band alignments in Pd/p^+(WSe_2)/n^+($SnSe_2$) heterojunction are simulated under different V_{ds}, and then the NDR behavior is explained based on the energy band diagrams (Figure 2). Here, it should be noted that the negative drain voltage is the forward bias and the positive drain voltage is the reverse bias because we contact the source electrode on the p-type WSe_2.

At the forward drain bias (V_{ds} < 0 V in Figure 2a, corresponding to region (i) in Figure 1d), electrons in the $SnSe_2$ conduction band tunnel to the WSe_2 valence band and then recombine with holes in the WSe_2 valence band, and thus the forward BTBT current is formed. At a small reverse drain bias (0 V < V_{ds} < V_{peak} in Figure 2b, corresponding to region (ii) in Figure 1d), electrons in the Pd electrode tunnel to the valence band in WSe_2 and then recombine with holes in the WSe_2 valence band, which are transported by BTBT at the WSe_2/$SnSe_2$ junction, resulting in the formation of the reverse BTBT current. Further increase of the drain bias (V_{peak} < V_{ds} < V_{valley} in Figure 2c, corresponding to region (iii) in Figure 1d) depletes the WSe_2 valence band near the WSe_2/$SnSe_2$ junction and reduces the BTBT current at the WSe_2/$SnSe_2$ junction. At the drain bias over the valley voltage (V_{valley} < V_{ds} in Figure 2c, corresponding to region (iii) in Figure 1d), no more BTBT current at the WSe_2/$SnSe_2$ junction exists and only the reverse thermionic emission (TE) current over the large Pd/WSe_2 Schottky barrier remains. The current saturation in this voltage region is due to the limited reverse TE of electrons over the large Pd/WSe_2 Schottky barrier. With application of a very high drain bias ($V_{valley} \ll V_{ds}$ in Figure 2c), electrons from the Pd electrode can be tunneled through the triangular WSe_2 conduction band by Fowler–Nordheim (FN) tunneling. It is not shown in the long WSe_2 channel (5 μm) device in Figure 1d but is shown in the short WSe_2 channel (1 μm) device in Figure 5e, which is also confirmed in the $\ln(I/V^2)-1/V$ plot (see Figure S6).[36] It is noteworthy that Pd/WSe_2 contact in our device has a much higher Schottky barrier than previous Cr/WSe_2 contact in the WSe_2/$SnSe_2$ device,[9] which suppresses the reverse TE current to less than the BTBT current level. Therefore, NDR behavior in our device can be shown at room temperature, while the previous Cr/WSe_2 contact device demonstrates only an NDR trend because the reverse TE current through the small Cr/WSe_2 Schottky barrier is larger than the BTBT current at room temperature. To conclude, the maximum current is manifested with resonant energy levels between two layers, and the current is finally reduced to saturation, followed by FN tunneling or thermionic emission to primarily dominate the current.

As $SnSe_2$ is highly sensitive to air and easily degraded during the conventional dry transfer process,[9] oxidative degradation to $SnSe_2$ would severely influence the interface quality, although WSe_2 is stable under ambient air conditions. The oxidation effect on $SnSe_2$ and WSe_2 flakes with exposure to ambient air over time was systematically studied. The optical microscopy (Figure 3a) and AFM (Figure 3b) images illustrate the surface morphological variations on exfoliated $SnSe_2$ with the appearance of small spots after 5 h of oxidation, which grow increasingly larger with time (denoted by white arrows in Figure 3a). The obvious spots aggregated on the surface are attributed to the faster oxidation at defect positions than other areas. Unlike the oxidation processes of BP flakes being etched layer by layer with an obvious decrease in thickness[37] and HfS_2 flakes becoming multiply thicker due to the intercalation of oxygen atoms between layers,[38] the $SnSe_2$ flake maintains its original thickness with a negligible increase (height profiles in Figure 3b). This is because a distinct oxidation process that affects the $SnSe_2$ surface with material transformation, revealed in the comparison of cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images and energy dispersive X-ray spectroscopy (EDS) element mappings (Figure 4a,b). For heterostructures in air, the upper part of the $SnSe_2$ flake retained its crystalline layer structure the same as the $SnSe_2$ flake manipulated in a glovebox without variation in element signals. Meanwhile, the lower part exhibits a disordered transformation into an amorphous layer. In the Raman spectra of the $SnSe_2$ flake measured at various exposure times (Figure 3c), an additional new peak near the representative vibration mode of the E_{2g} peak (fitted using the Lorentz model) started to appear after 1 h of oxidation. With a further increase of the exposure time, the new peak became more apparent and completely dominated over the E_{2g} peak after 24 h of oxidation. This new peak agrees with the phonon mode of $SnSe_{2-x}$[39,40] rather than the Sn_xO_y, corresponding to the evident decrease of the Se signal and the lack of O signal that was observed in the EDS analysis. Electrical stability of $SnSe_2$-FET was characterized by repetitively measuring its transfer curves over time, where I_{ds} exhibits a decrease of approximately 1.6 times after 7 days in air (Figure 3d). In contrast, the WSe_2 flake maintains both a consistent surface morphology and Raman spectra throughout the measurements (see SI Figure S7), suggesting the strong structural stability against ambient air. Simultaneously, the electrical performance of WSe_2-FET shows an identical current level for over 7 days to the air exposure. In summary, $SnSe_2$ flakes are sensitive to ambient air and are easily oxidized without effective protection, leading to the degradation of both the chemical structure and electrical properties. WSe_2 flakes possess a robust ability to resist the destruction of ambient air conditions, coinciding with results reported in previous literature.[41]

To explore the influence of heterointerfaces in an NDR diode, WSe_2/$SnSe_2$ devices fabricated in air and inert gas are systematically studied for comparison. The cross-sectional TEM image of the device in air exhibits disordered layers at the interface with a thickness of ~2.4 nm (Figure 4a). In contrast, the TEM image of the devices in inert gas clearly resolves both WSe_2 and $SnSe_2$ layers, as well as the more distinct interface (Figure 4b). Benefiting from our well-developed dry transfer method utilized inside the glovebox, there was no additional oxidation layer or typical vdW gap, resulting in an ultrasharp and clean interface. Devices fabricated in air and inert gas are electrically characterized to explore variations in NDR behavior (Figure 4c). The peak and valley currents are typically observed with tunneling, followed by the FN tunneling at high voltage. Moreover, the device fabricated in a glovebox exhibits high NDR performances, with a higher tunnel current and peak-to-valley ratio than those fabricated in air. The peak current of 23 mA/mm^2 is 2 orders of magnitude higher than that in air (0.22 mA/mm^2) and the peak-to-valley ratio is 1.8, compared to less than 1.5 in air; however, these values varied between samples. This difference is attributed to the oxidation layers formed in ambient air, which would provide numerous traps or recombination sites and serve as a tunneling barrier, greatly affecting NDR performance. Meanwhile, the devices fabricated inside the glovebox contain minimal oxidation layers, presenting relatively high and stable tunneling currents

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of 20−30 mA/mm^2 and peak-to-valley ratios of 1.8−2.2. These results imply that the quality of the heterointerface plays a key role in the performance of tunneling devices.

To further improve NDR performance, 2D hexagonal boron nitride (h-BN) layers are used as the gate dielectric to reduce the trap scattering and stain effects, as well as to provide high gate-effect efficiency, by substituting the SiO_2 dielectric.[42] An Esaki diode is constructed on the h-BN layer with monolayer graphene serving as the back-gate electrode (Figure 4d, and for the fabrication process and characterization, see SI Note 8 and Figures S8 and S9). The usage of an h-BN dielectric improves the peak-to-valley ratio to 4.0 by approximately 2 times and the peak current density up to 1460 mA/mm^2 (Figure 4e) by 2 orders of magnitude compared to that on a SiO_2 dielectric. Our device exhibits the highest peak current density among 2D materials-based NDR tunnel devices, exceeding over 3−4 orders of magnitude,[6,7,31,32] and also exhibits a relatively high peak-to-valley ratio (Figure 4f). This is a demonstration to date that the high performance of NDR tunnel devices based on 2D vdW heterostructures at room temperature is comparable to those of Si or Ge homo- or heterojunctions.[43−48] Besides, our device with h-BN encapsulation shows a negligible change in $I_{ds}-V_{ds}$ characteristics after 14 days of air exposure (see Figure S10). Since the current at the heterojunction has a tunneling component, the device can also work as a tunneling FET. The transfer characteristic (see SI Note 10 and Figure S13) shows a low subthreshold swing (SS) of 90 mV/dec for a current range of 5 orders of magnitude in the p-type region of the WSe_2/$SnSe_2$ TFET. It is noted that the SS in the TFET is usually improved by decreasing the thickness of the gate oxide or by adopting high-κ dielectrics as the gate oxide, according to the basic formulation of the tunneling probability for TFETs, which is displayed as[9]

$$T(E) \propto \exp\left[-\frac{8\pi\sqrt{2m^*E_g^{3/2}}}{3qh(E_g + \Delta\text{Ø})}\sqrt{\frac{\varepsilon_c}{\varepsilon_{ox}}t_c t_{ox}}\right] \quad (1)$$

where m^* is the electron effective mass, E_g is the band gap, h is Planck's constant, ΔØ is the energy range of feasible tunneling, and ε_c, ε_{ox}, t_c, and t_{ox} are the dielectric constants and thicknesses of the channel and gate oxide materials, respectively.

In our devices, the h-BN gate insulator layer is used to improve the peak current density and peak-to-valley ratio. By integrating the TMD heterostructure on the h-BN substrate of atomically flat and ultralow impurities, the peak current of the NDR diode can be increased by reducing the TMD roughness, trapped charges, and substrate surface phonons.[49] The improved carrier transport properties in the individual layer are shown in SI Note 9 and Figures S11 and S12. Furthermore, the valley current can be decreased by reducing traps in the forbidden gap of TMD generated from substrate-bound impurities at the channel−dielectric interface,[50] thereby suppressing the excess tunneling current through the traps in the TMD band gap. Nonetheless, the dielectric constant of h-BN is about 3.12,[51] which is significantly smaller than that of high-κ dielectrics such as Al_2O_3 (9.0−10.1) in a previous report.[9] This results in a high SS (90 mV/dec) in our TFET compared to previous work (37 mV/dec). Currently no high-κ 2D insulators are found to our knowledge, and therefore, it is difficult to achieve both high peak-to-valley ratio and low SS. Introducing high-κ gate dielectrics such as Al_2O_3 or HfO_2 by taking into account the removal of traps requires further study.

In previous reports, the uncertain quality of naturally formed oxidation layers is a crucial issue that impedes us from studying the insulating tunneling barrier effect on the NDR behavior. To study NDR performance depending on the thickness of the oxidized $SnSe_{2-x}$ layer as a tunneling barrier, we instead insert the h-BN layer with various thicknesses of 0, 0.34, 1.02, and 3.98 nm at a clean WSe_2/$SnSe_2$ interface (Figure 5a, and for fabrication process and characterization, see SI Note 11 and Figures S14 and S15).[52,53] As the h-BN thickness increases, both the peak current and peak-to-valley ratio are reduced (Figure 5b,c), indicating the decrease of the BTBT current. The BTBT current through the insulating barrier is decreased by direct tunneling (DT) probability, which is approximately estimated by[54]

$$T(E) = \exp\left[\frac{-4\pi W\sqrt{m^*\varphi_B}}{h}\right] \quad (2)$$

where W and φ_B are the width and height of the tunneling barrier, h is the Planck constant, and m^* is the electron effective mass. Direct tunneling probability along the h-BN thickness and BTBT conductance ($G_{BTBT} = I_{BTBT\_peak}/V_{peak}$, where $I_{BTBT\_peak} = I_{total\_peak} - I_{diffusion}$ in Figure 5b) at h-BN thicknesses of 0, 0.34, 1.02, and 3.98 nm is plotted in Figure S16. The tunneling probability gradually decreases as the tunneling barrier width enlarges, which clearly matches with the reduction of BTBT conductance. Therefore, the NDR performance of the device is gradually degraded as the h-BN barrier width increases. Following this tendency, the NDR device possesses an inferior performance and low tunneling current if the oxidation layer is thicker than 1 nm, which is also well proved by our devices fabricated in air. When the oxidation layer is more than 4 nm, it is considered that the devices would lack NDR behavior, which is frequently reported by others with the same device structure.

Practically, the source−drain current contributed by the FN tunneling or thermionic emission falls dramatically with a decreased temperature, whereas the BTBT current shows an opposite trend. The temperature-dependent $I_{ds}-V_{ds}$ curves were acquired at 300, 250, 190, 170, and 145 K (Figure 5d) at a back gate of −90 V. Our device maintains the NDR behavior regardless of temperature decrease and exhibits an increased peak current, confirming a BTBT mechanism. At low temperature, the Fermi−Dirac distribution curve becomes closer to the Fermi level, enhancing the probability of energy states near the Femi level being occupied by electrons. This eventually increases the BTBT current since the filled states are increased below the $SnSe_2$ Fermi level while having more empty states in WSe_2. Another apparent feature is the slightly positive shift of peak voltage at low temperature, attributed to the increase in contact resistance at the metal−semiconductor junction.[55] Besides, the peak-to-valley ratio increased from 1.05 (300 K) to 1.33 (145 K) (inset in Figure 5d) with a decreased current after the valley point, showing a similar trend to that observed in other 2D semiconductor-based NDR devices.[6,31]

NDR performance is further tuned *via* electrostatic gating (Figures 5e,f), which starts to appear while being gated at −70 V. At a high negative gate voltage, *i.e.*, $V_g < -70$ V (see Figure S17a), the WSe_2 layer accumulates hole carriers, resulting in

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the BTBT taking place from Pd to the $SnSe_2$ conduction band through the WSe_2 valence band. Therefore, NDR behavior occurs in this gate voltage region. Meanwhile, at a lower negative gate voltage, *i.e.*, $V_g > -70$ V (see Figure S17b), BTBT through the WSe_2 valence band is not allowed. As a result, the source−-drain current is contributed by the thermionic emission from Pd to the WSe_2 conduction band, and then the NDR behavior does not appear in this gate voltage region. Gate-tunable NDR behavior becomes more prominent with increased peak current density by more than 10 times at −100 V, as well as the increased peak-to-valley ratio, where the Fermi level in the WSe_2 layer moves further from its valence band, leaving more available empty states.

CONCLUSION

We have demonstrated that the quality of the vdW heterointerfaces is crucial to achieve high tunnel device performance. Since $SnSe_2$ is an air-unstable material, a glovebox dry transfer method is well developed to construct the $SnSe_2/WSe_2$ heterojunctions, which efficiently suppressed the oxidation layers at the heterointerfaces, ensuring the generation of a pure and clean channel for the interband electron tunneling transport. Besides, Pd/WSe_2 contact in our device possesses a much higher Schottky barrier than previously reported Cr/WSe_2 contact in the $WSe_2/SnSe_2$ device, which suppresses the thermionic emission current to less than the BTBT current level, enabling the clear observation of NDR at room temperature. Hence, the realization of an NDR device with an extremely high tunneling current density of 1460 mA/mm^2 and a high peak-to-valley ratio of 4 has been shown, which is the highest value among conventional 2D materials-based NDR devices and comparable to 3D devices. In addition, by exploring the influence of the heterointerface in the NDR diodes, we experimentally discovered that the tunneling barrier could degrade NDR performance. Moreover, our devices also exhibit an efficient tunability of NDR performance by electrostatic doping. They therefore suggest promising possibilities for future low-power electronics.

METHODS

Device Fabrication. The bottom-up assembly method was employed with series of combined wet bubbling transfer (for CVD flakes), glovebox PPC dry transfer (for $SnSe_2$ flakes), and traditional PMMA dry transfer (for exfoliated flakes). The glovebox system for heterostructure fabrication was equipped with an optical microscope and dry transfer system. The O_2 and H_2O concentrations inside were maintained at less than 1 ppm by circulation with high-purity argon gas. Detailed processes can be found in SI Notes 1, 8, and 11, respectively.

Characterization. Witec Raman spectroscopy (532 nm laser) was used to study Raman spectra of the samples. The AFM mapping analyses were recorded in a SPA400 (SEIKO) system. Electrical transport measurements, including temperature-dependent characterization, were carried out with a probe station and source/measurement units (Keithley 4200 and Agilent B2900A) under high-vacuum conditions (10^{-6} Torr).

Electronic Band Structure Calculation. First-principle calculations based on density functional theory (exchange−correlation function) were performed to calculate the band gaps of WSe_2 and $SnSe_2$ with three layers. The detailed calculation process can be found in SI Note 3.

Band Alignment Simulations. The charge distribution based on Poisson's equation was solved in MATLAB. Detailed simulation equations, parameters, and results are provided in SI Note 5.

Fitting of Source−Drain Current. The carrier transport mechanism of band-to-band tunneling was considered for the fitting in MATLAB in SI Note 6.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.9b03342.

Notes 1−11 and Figures S1−S17 contain the fabrication processes and characterizations of devices, DFT simulations for band structures, band alignment simulations using Poisson's equation, fitting equation for band-to-band tunneling current, the $\ln(I/V^2)-1/V$ plot of FN tunneling and thermionic emission, the stability of devices against air ambient, carrier transport properties in WSe_2-FET on an h-BN dielectric, tunneling field effect in the $WSe_2/SnSe_2$ heterostructure (PDF)

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Notes

The authors declare no competing financial interest.

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